

ABSTRACT

5 A wireless (radio) receiver receives RF signals carrying
data synchronized with a first clock. The wireless receiver
demodulates the RF signals to extract the data signals and the
first clock signals. The wireless receiver uses the first
clock signals as write signals to write the data signals in a
10 first-in first-out memory device (FIFO). The data signals
stored in the FIFO may be read out with read signals
synchronized to a second clock. In one example, a host
associated with the wireless receiver reads out data signals
stored in the FIFO with read signals synchronized to the
system clock of the host receiver. In another example, the
15 wireless receiver includes a data processing circuit (e.g.,
including forward error correction, de-whitening, and cyclical
redundancy check circuits) that reads out data signals stored
in the FIFO with read signals synchronized to the system clock
of the wireless receiver.

20 A microprocessor system architecture is disclosed which
allows for the selective execution of programmed ROM microcode
or, alternatively, RAM microcode if there has been a
correction or update made to the ROM microcode originally
programmed into the system. Patched or updated RAM microcode
25 is utilized or executed only to the extent of changes to the
ROM microcode, otherwise the ROM microcode is executed in its
normal fashion. When a patch is received, it is loaded into
system RAM along with instructions or other appropriate
signals to direct the execution of the patched or updated
30 microcode from RAM instead of the existing ROM microcode.
Various methods are presented for selecting the execution of
the appropriate microcode depending upon whether there have
been changes made to it.

SDB/cah

35 CAH PAS528925.1-*--09/30/03 9:22 AM